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19 January 2025

High-Density Resistive Switching Devices Fabricated by Block Copolymer Self-Assembly

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KEYWORDS resistive switching, ReRAM, high-density array, HfO_2, cross-talk, bottom-up fabrication, block copolymer, self-assembly

ABSTRACT Bipolar resistive switching memories based on metal oxides offer a great potential in terms of simple process integration, memory performance, and scalability. In view of ultra-high-density memory applications, a reduced device size is not the only requirement, as the distance between different devices is a key parameter. By exploiting a bottom-up fabrication approach based on block copolymer self-assembling, we obtained the parallel production of bilayer Pt/Ti top electrodes arranged in periodic arrays over the HfO_2/TiN surface, building memory devices with a diameter of 28 nm and a density of $5 \cdot 10^{10}$ devices/cm^2. For an electrical characterization,

the sharp conducting tip of an atomic force microscope was adopted for a selective addressing of the nanodevices. The presence of devices showing higher conductance in the initial state was directly connected with scattered leakage current paths in the unpatterned oxide film. With bipolar voltage operations, we obtained reversible set/reset transitions irrespective of the conductance variability in the initial state, and the high density of the produced electrodes allowed us to detect a cross-talk between different devices occurring during both set and reset transitions, which poses a scalability issue for ultra-high density memory applications.

INTRODUCTION

Bottom-up nanofabrication approaches based on block copolymer (BCP) self-assembly offer the possibility to generate high-density features at nanoscale.[1,2] The exploitation of this key-enabling technology for the fabrication of high-density arrays of nanostructured resistive switching devices has not been investigated in detail. Indeed, resistive switching memories (ReRAM) are among the main candidates for future solid-state memory applications able to satisfy the increasing demands in terms of data storage capacity, low power consumption and fast accessing time.[3–5] Resistive switching (RS) devices consist of two terminals capacitor-like structures in which the electrical resistance of the system can be reversibly switched between two (or more) non-volatile values with the application of a potential difference between the two metal electrodes.[6] In a variety of materials, the RS mechanism can be explained in terms of formation of a filamentary conductive path bridging the two electrodes in the low resistance state (LRS) during the set operation, while in the reset process the filament is partially disrupted, leading to the high resistance state (HRS).[7,8] Usually, the switching is initiated by a unique forming process which is responsible for the first establishment of the conductive filament. Due to the small filament size, filament-based RS memories are particularly suited for scaling. In particular, transition metal oxides are among the

main candidates as dielectric materials in future RS memories.[9] HfO_2 is increasingly becoming a model example, since it offers excellent CMOS process integration capability and promising memory performances.[10,11] Recent reports revealed sub-10 nm conductive channel diameter in HfO_2-based RS devices[12,13] and well-functioning nanoscale devices have been fabricated using either electron beam lithography or a three-dimensional stacking procedure.[14–16] However, these fabrication methods allow the definition of a limited number of memory cells, while the scalability limit of high-density packing has not been explored.

In this view, block copolymer (BCP) thin films demonstrated the ability to self-assemble in periodic nanodomains that can be exploited for the fabrication of nanoscale features, often in combination with current top-down patterning technologies.[1,17,18] This high throughput patterning technique offers the advantage of producing ultra-high density devices, yet maintaining a good control over the device size and spacing as a function of the polymer molecular weight.[19,20] BCPs allow the definition of regular patterns with dimension and spacing that easily go beyond the limits of current optical lithography[21], and have been used for the formation of complex patterns in different applications such as FinFET transistors, circuit interconnects, capacitors, and charge trapping memories.[22–24] BCPs have also been employed in the fabrication of phase change memories for a reduction of the electrode contact area, achieving a significant power reduction.[25] RS device top electrode downscaling using BCP in combination with electron beam lithography has been reported, in which the BCP was applied to define narrow but isolated features.[26]

In this work, we employ a BCP-assisted lithographic process for the parallel fabrication of nanosized, high-density metal electrodes organized in regular arrays over the HfO_2 switching material. With the conductive tip of an atomic force microscope (C-AFM), we achieve a selective

addressing of the single nanodevices, in order to obtain the switching phenomenon at the nanoscale and investigate the effect of density upscaling on the system properties.

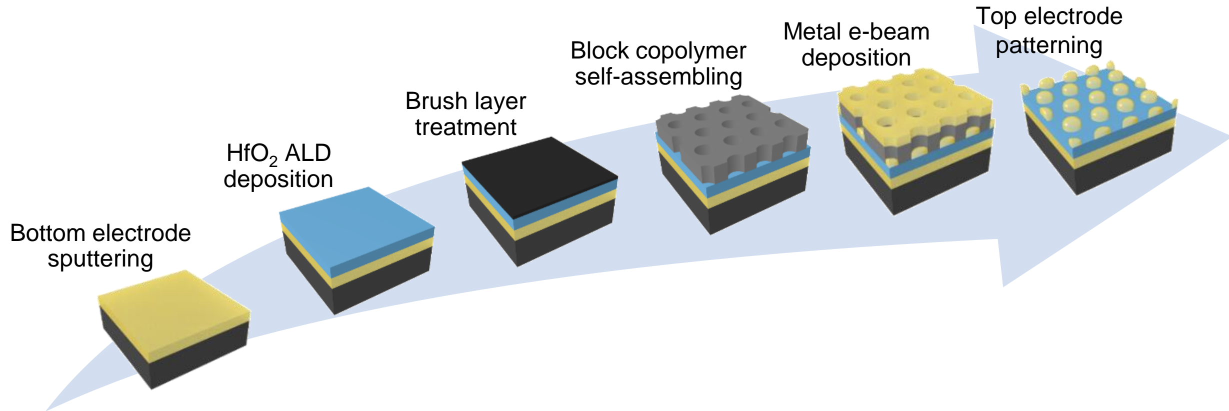

Figure 1. Procedure for the top electrode patterning. A BCP self-assembled template was adopted for pattern transfer with a lift-off process.

RESULTS AND DISCUSSION

Fabrication of nanoscale RS devices with BCP template

Figure **1** summarizes the adopted process workflow to obtain an ordered array of RS devices by BCP lithography. The first step consists in the sputter deposition of the TiN bottom electrode, followed by the atomic layer deposition (ALD) of a 3 nm HfO_2 film and finally by the Pt/Ti top electrode nanopatterning. This final step employs a lift-off process with a nanoporous template formed by BCP self-assembling.[19,20,27,28]

Before BCP deposition, the oxide surface was functionalized with a brush layer of P(S-*r*-MMA) random copolymer, which is necessary in order to remove the poly(methyl methacrylate) (PMMA) preferential wetting of the surface and obtain a perpendicular orientation of the cylindrical nanodomains in the above BCP layer.[29,30]

The BCP phase separation was induced with a rapid thermal processing (RTP) heat treatment that allowed a short processing time of 5 minutes.[31,32] We employed a PS-*b*-PMMA block copolymer with PS content of 70%, obtaining PMMA cylindrical nanodomains with hexagonal periodic distribution within the polystyrene (PS) matrix. Upon selective removal of the PMMA polymeric component, a nanoporous PS periodic structure was obtained, as shown in the SEM image of Figure **2**a. The BCP lithographic technique offers the possibility of a fine tuning of the device size and spacing as a function of the polymer molecular weight (M_w).[33] By employing a M_w of 102 kg/mol, we obtained devices with a diameter of 28±1 nm and 47±1 nm center-to-center distance, which resulted in an average spacing between neighboring devices of 19±1 nm and a density of $5x10^{10}$ devices/cm^2. The Pt/Ti top electrode was electron-beam deposited through the nanoporous template, and a solvent-assisted lift-off process was adopted to produce the ordered arrays of nanopatterned top electrodes shown in the SEM image of Figure **2**b. We deposited in this step a bilayer structure composed of 4 nm Ti and 6 nm Pt, obtaining the device structure descripted in Figure **2**c. The Ti layer was chosen because of his oxygen-reacting property, which was demonstrated to significantly reduce the forming voltage and reduce the device variability.[34,35] Figure 2d shows the sample surface morphology obtained by AFM, where distinct nanodevices with hexagonal distribution are clearly distinguishable. In Figure **2**e, a line scan extracted from Figure **2**d is shown. The average electrode height of 8±1 nm obtained from AFM data analysis is compatible with the deposited metal thickness, while the electrode size appears larger than in the SEM image (Figure 2b) because of the lateral convolution with the AFM tip geometry.

Due to the oxidation of the TiN upper interface prior to the HfO_2 deposition, an additional TiO_2 oxide layer of roughly 2 nm intermixed with TiO_xN_y components was found by XPS analysis (data not shown). This additional oxide layer was reported to increase the LRS resistance, which is

desirable for large array memory architectures.[15] This highly defective interface can additionally accommodate excess oxygen species during the set process, serving as oxygen reservoir for the filament oxidation in the subsequent reset process.[36] Besides, the deposition of a thin 3 nm HfO_2 was chosen in order to lower the operation voltages, as required for RS device scaling.[37,38]

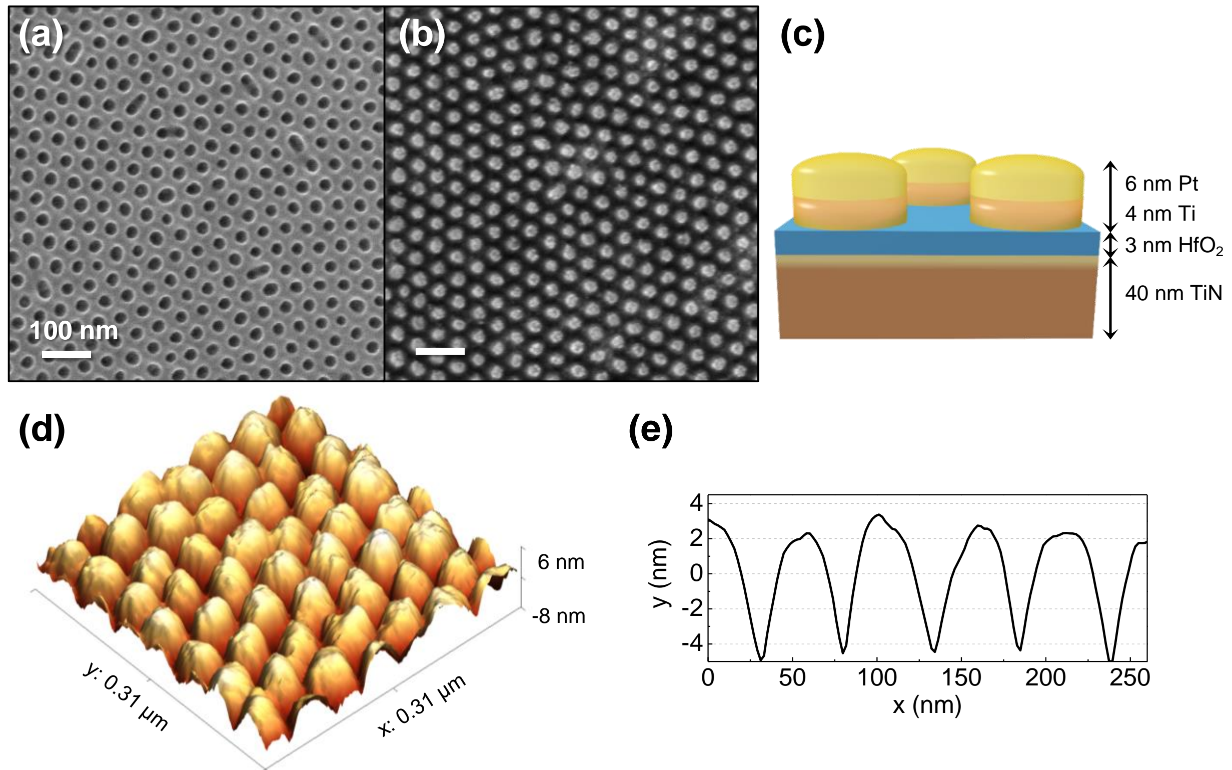

Figure 2. SEM plane views of (a) nanoporous PS template obtained by BCP self-assembling in periodic perpendicular cylinders and (b) arrays of Pt/Ti top electrodes on top of the HfO_2 surface obtained from the self-assembled polymeric template depicted in (a). (c) Device stack representation. (d) AFM surface morphology showing the top electrodes with hexagonal distribution and relative line scan (e) displaying the electrodes height.

Initial state characterization of the nanoscale devices

Figure 3a and 3b display simultaneously acquired C-AFM topographic and current maps for the characterization of the initial leakage conductance of the devices. A potential difference of 1.5 V

was chosen to highlight the device variability, yet low enough to avoid electric field-induced perturbations, as verified with repeated scans. A close correlation can be found between the hexagonally packed Pt/Ti metal electrodes in Figure 3a and the uniform conductive spots in Figure 3b, confirming the equipotential behavior of the nanometer-sized metal electrodes, which is the first requirement for their correct operation. We noticed however very different leakage current levels among different devices. By plotting the cumulative distribution of the initial state resistances, two different conditions can be defined in Figure 3c. While nearly 80% of the devices with higher resistance show a very low dispersion, around 20% of the remaining devices in the lower resistance distribution tail have a conductance spread over almost 2 decades. Repeating the initial state analysis in a different area of the sample and with a different voltage, the same general trend was obtained (Figure S1).

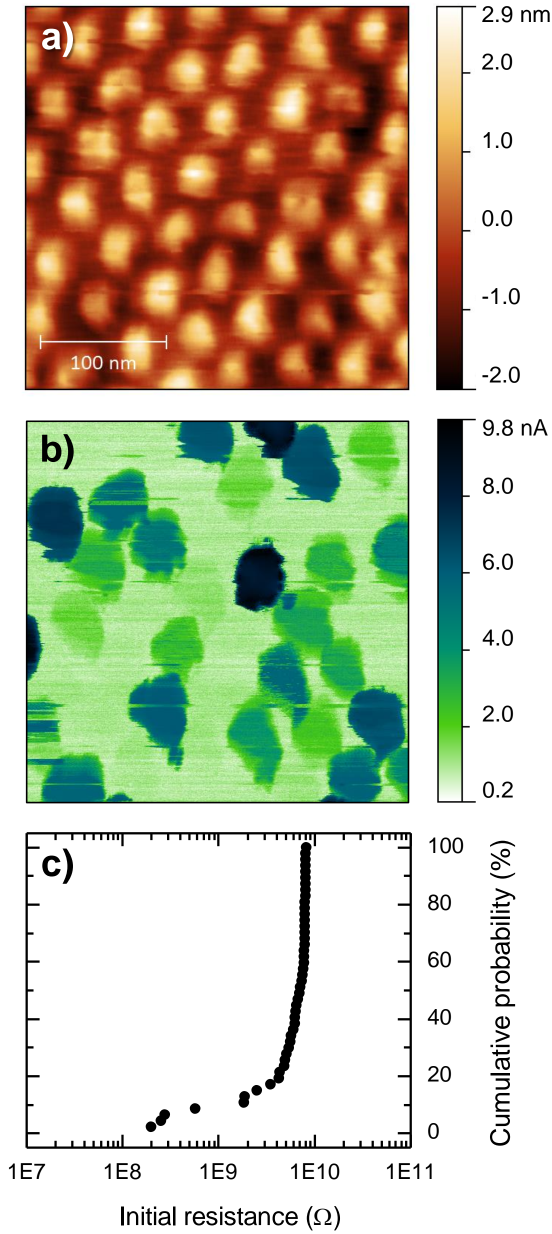

Figure 3. AFM morphology (a) and corresponding current map (b) of top metal electrodes defined by BCP lithography on the HfO_2 surface, acquired with an applied bias of 1.5 V. (c) Initial state resistance distribution of the devices in figure (b).

In order to investigate the device initial state variability, we assessed the oxide non-homogeneity at the nanoscale by acquiring current maps of the bare HfO_2/TiN film surface, before top electrode patterning, using the conductive AFM tip as top electrode (Figure 4). The majority of the HfO_2

film is highly insulating and presents a leakage current below the detection limit. This finding correlates well with the 80% of highly resistive devices reported in Figure 3. Additionally, leaky sites in HfO_2 are randomly spread, with a current level that differs greatly between the different sites.[39] This is likely the cause of the resistance variability over 2 decades for the 20% of the most conductive nanodevices, probably located in correspondence of leaky conduction paths. This C-AFM electrical characterization of the bare oxide is in agreement with what is in general observed for amorphous 3 nm HfO_2 samples.[40,41] We observed an average number of 100 spots/μm^2 at 1.5 V, a value in agreement with previous observations[40]. Comparing this value with the density of 500 devices/μm^2 in the sample with BCP patterned electrodes, we can clearly correlate the 20% of highly conductive devices with the inherent presence of leakage current paths in the bare HfO_2/TiN stack.

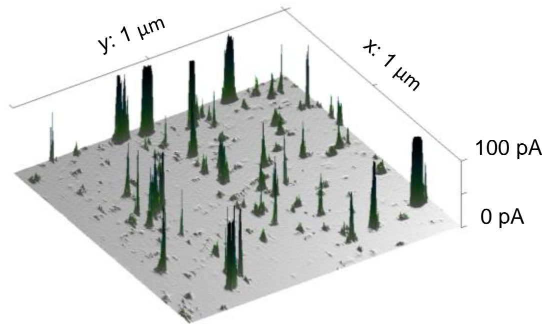

Figure 4. C-AFM current map of a 3 nm HfO_2/TiN bare surface acquired at 1.5 V bias displaying the film nanoscale conductance variability.

Nanoscale device RS operations

With the sharp conductive tip of the AFM, we achieved a selective addressing of individual nanoscaled memory cells. By placing the tip over a selected electrode and ramping the voltage, the forming transition can be obtained (Figure 5a). We repeated the operation on different randomly

selected devices, finding forming voltages comprised in the 4.5 – 5.5 V range. This transition can be obtained regardless of the device initial resistance status, meaning that the inherent presence of leakage conduction paths is not a prerequisite for the device forming. When using a direct AFM tip contact (Pt-Ir coated tip as top electrode), previous works on 3 nm HfO_2 amorphous films point out that quite a high voltage (>16 V) is necessary to induce the oxide breakdown.[40,41] Indeed, acquiring voltage scans over the HfO_2/TiN bare surface in 25 random positions, no forming transition in the 0 – 10 V range was obtained, locating the tip in areas showing either leaky sites or low initial conduction (see Figure S2). In comparison with a direct AFM tip contact, the nanoscale electrical characterization of the RS system using nanoelectrodes defined by BCP lithography brings the big advantage that real devices are investigated. In this way, various artifacts located at the oxide – electrode interface can be avoided (water meniscus, anodic oxidation, etc.),[42] while the device area can be carefully defined by the BCP template and the electrode material can be more easily selected. In this respect, the insertion if the Ti interlayer in the top electrode stack allowed to exploit the Ti oxygen scavenging effect, which was previously associated with a visible reduction of the forming voltage.[34,35,43]

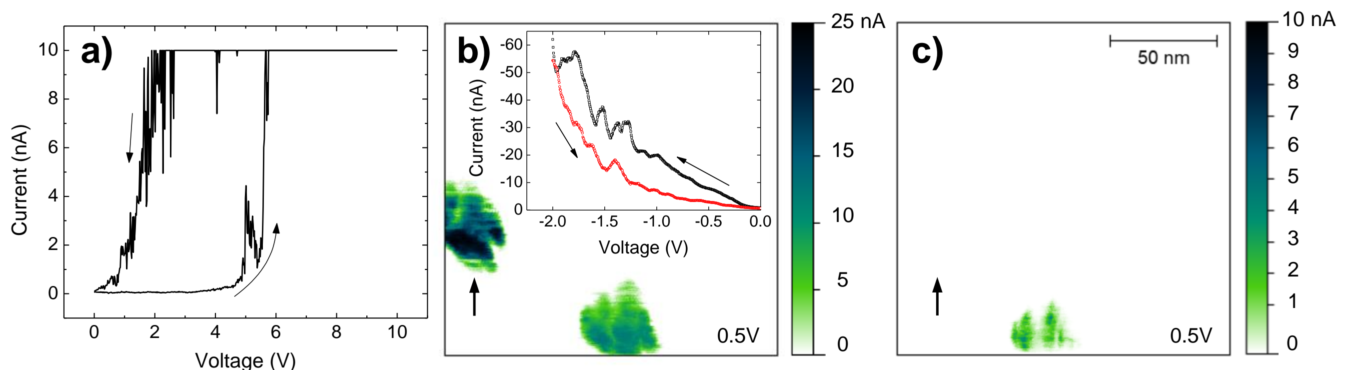

Figure 5. High initial resistance device (a): Forming process in a Pt/Ti/HfO_2/TiN nanodevice. 10 nA is the maximum detectable current. Initially leaky devices (c) and (d): Current maps acquired

at 0.5 V before and after the reset operation (inset) of the device indicated by the arrow. After reset, this device is not anymore visible in the reading current map (d).

Considering devices located in correspondence of leaky sites, their higher initial conductance can be manipulate with bipolar voltage operations. In Figure 5b, a current map acquired at 0.5V shows in the scanned area two devices with high initial conductance. Selecting the device indicated by an arrow and performing a steady state negative voltage sweep (inset of Figure 5b), the device conductance is suppressed, as it is evident in the subsequent reading current map of the same area (Figure 5c). This can be interpreted as the reset of a device that is initially in a LRS, with the conductive channel already in place without the requirement of an initial forming step.

Owing to the small electrode dimension, which is of the same order of magnitude of the tip contact area, a different C-AFM procedure was developed to gain better reproducibility during repeated set/reset processes. By scanning the tip over only one selected device with a constant applied bias, we improved the tip – electrode contact, while the applied bias was chosen high enough to induce the RS phenomenon. The induced conductance modification was then inspected with a following reading current map over a larger area at a low non-perturbing voltage. The result of this switching procedure is reported in the series of reading current maps of Figure 6. In Figure 6a, a current map displays the initial resistance status of the devices. The AFM tip was then scanned with a constant bias of +4 V over the area enclosed by the black square (50 nm side), containing a single device which exhibits an initial current level below the ammeter sensitivity but was visible in the related topographic map (not shown). The subsequent current map of the whole area (Figure 6b) shows a significant conductance increase of the device under test (forming process). The voltage required to induce the forming transition was is in this case slightly lower than that required for punctual AFM tip operations as in Figure 5a, thanks to the longer lasting

voltage stress induced with scanning tip operations, along with a more stable tip – electrode contact that helps reducing the contact series resistance. Scanning again over the same device with -3V, we substantially suppressed the conductivity (reset), as visible in Figure 6c, while with the application of +4 V we were able to restore the low resistance state (Figure 6d). It is worth noting that the reading current maps were acquired about 10 minutes after the switching occurred, indicating a non-volatile switching in resistance.

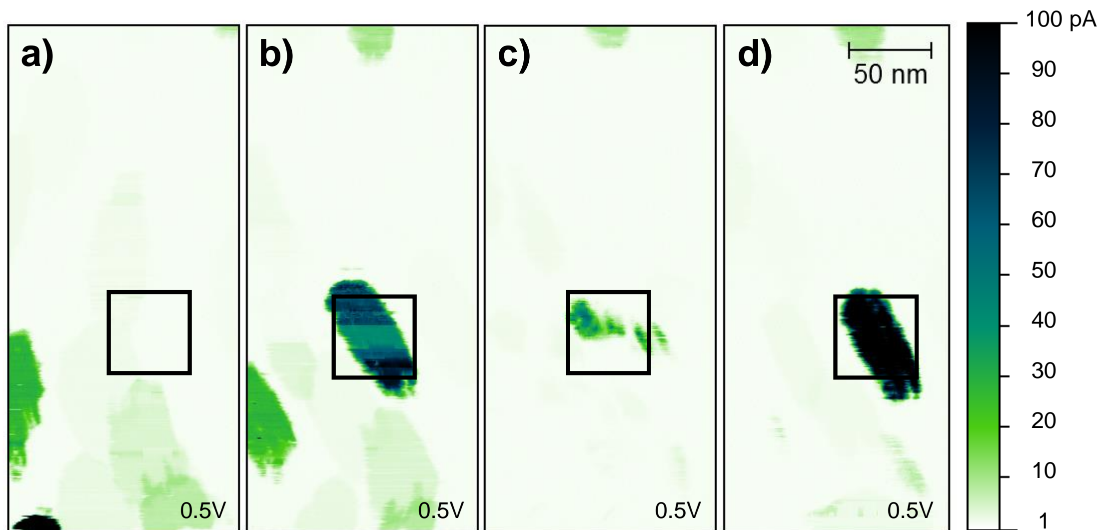

Figure 6. Current maps (0.5 V bias) acquired before the switching processes (a), after the set process with +4 V (b), after reset with -3 V (c), and after set with +4 V (d). The black square, containing a single nanodevice, encloses the area where the tip was scanned with +4 V/-3 V to induce the set/reset transitions. The elongated shape of the metal electrodes is an artifact caused by a drift in the scanning system.

The same operation was also performed in the series of current maps reported in Figure 7 on a device that exhibited a not negligible initial state leakage current, as evident in Figure 7a. However, we noted that after the application of +4 V to the area enclosed by the black square, in Figure 7b we were able to increase the device conductivity to a level comparable with the one of the device

selected in Figures 6b and 6d, regardless of the initial device variability. Moreover, by applying -4.5 V, we were able to annihilate the conduction path and reach a resistance value lower than the initial state, with a final current value under the detection limit (Figure 7c). The complete reset highlights the high control on the HRS that can be attained with nanosize devices, which is at the basis of the ON/OFF window opening previously observed in nanoscale systems.[38]

In Figure 7, another interesting aspect is visualized. The two conductive devices on the left side of Figure7a, even if not nearest neighbors, share the same initial current value of 15 pA. After the application of a potential difference to the device enclosed by the black square, the not selected device at the bottom left was also influenced. This cross-talk effect between distinct devices at a distance of 75 nm was obtained again during the reset operation, when both devices reached a resistance value higher than the initial state. It is worth noting that another device is located in between the considered electrodes, which was unaffected during both set and reset operations, demonstrating that the observed cross-talk cannot be ascribed to the tip contacting neighboring devices at the same time. Two other devices visible in Figure 7 at a distance of 80 nm and 130 nm were also unaffected, while a slight lowering in their conductance from Figure 7a to Figure7c can be ascribed to the tip coating wearing out.

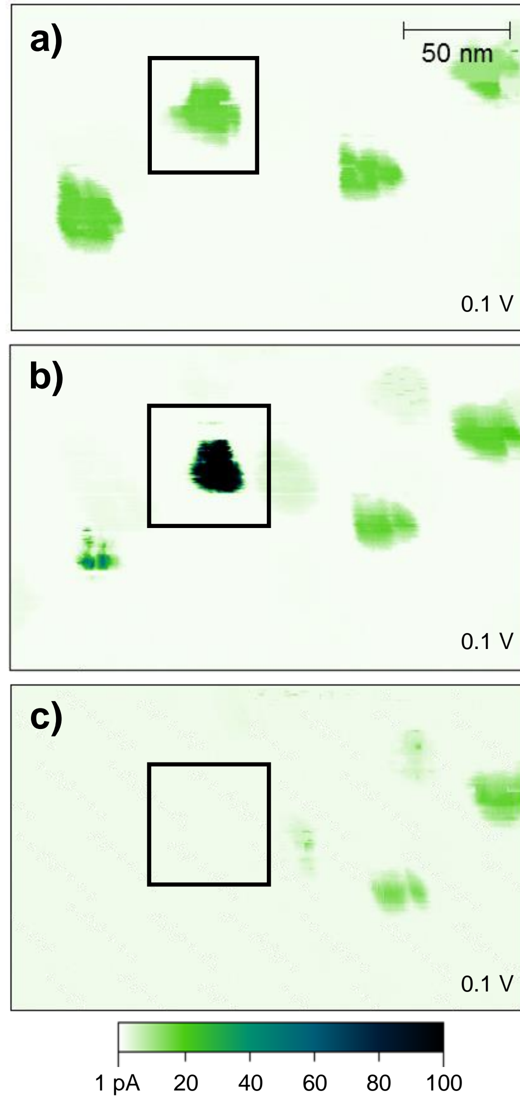

Figure 7. Current maps (0.1 V bias) acquired before the bipolar voltage operation (a), after set (b), and after complete reset (c). To induce the set and reset processes, the tip was scanned in the area enclosed by the black squares with a constant applied bias of +4 V (set) and -4.5 V (reset).

A similar cross-talk phenomenon was previously reported in the bare HfO_2/TiN stack using the conducting AFM tip as a mobile top electrode scanning the surface. After forming, distinct conductive spots appeared in the scanned region, while the afterward reset of one spot influenced the neighboring ones. The observed phenomenon was explained with the formation of bunches of

connected conductive filaments during forming.[39] In the present case, we adopted an array of fixed devices instead of a mobile scanning electrode, with the AFM tip contacting only one device during forming. The presence of connected filaments should therefore be intrinsic of the HfO_2/TiN stack, as also indicated by the reinforcement of both devices after forming in Figure 7b.

DISCUSSION

Starting from the experimental evidences, we propose a model to explain the observed phenomenon. In Figure 8, we relate the line scans of the correlated devices (snapshots of the current maps of Figure 7 are reported as insets) with a pictorial view of the proposed model. Starting from Figure 8a, since the two devices show an initial conduction level higher than the neighboring devices, there must be leaky conductions path already in place in the HfO_2 film. As a positive potential difference is applied between the common bottom electrode and the selected top electrode (Figure 8b), the filament gets reinforced due to oxygen vacancies formation and migration in the filament region[44,45]. Since this process leads to a conductance increase of both the selected and unselected devices, they are likely to share a common portion of the filamentary conduction path. The final current level of the not selected device is however lower than that of the selected device, meaning that only a small branch of the filament is shared. When a negative voltage polarity is applied (Figure 8c), a gap is created in the filament region as oxygen vacancies migrate toward the bottom electrode and the filament is oxidized, interrupting the conduction path for both the considered devices.

Even if the experimental results suggest the existence of connected filamentary conduction paths, their exact localization is not straightforward. As suggested by Brivio *et al.*[39], the origin of the localized conduction paths can be located at the highly defective HfO_2/TiN interface, with the TiN surface roughness also likely to play a role. Even though the filaments should extend

throughout the oxide film thickness, its amorphous structure excludes the presence of grain boundaries as fast diffusion paths for the oxygen vacancies, leaving room for additional investigations in order to get a further comprehension of the described phenomenon.

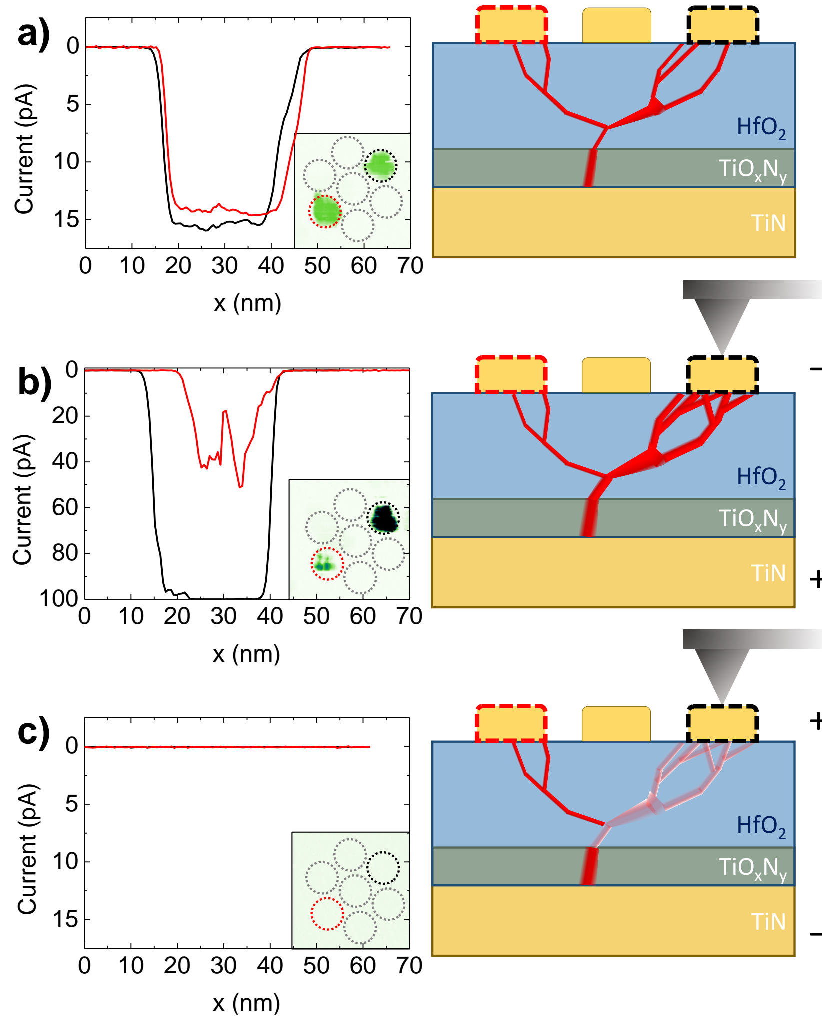

Figure 8. Schematic model of the correlated switching for two different devices. Three top electrodes are represented, being part of a periodic electrodes array with hexagonal distribution, as represented in the insets of (a)-(c) with dotted circles. On the left, line scans of the device to which the bias was applied (black) and of the other correlated device (red) before the bipolar voltage operations (a), after set (b), and after full reset (c). On the right, a pictorial view illustrates the proposed cross-talk mechanism.

Thermal profile simulations recently pointed out the thermal cross-talk, rather than the filament size itself, to be the ultimate limit for device scaling.[46] We however can exclude thermal cross-talk to be the cause of linked switching behavior in our system. Indeed, a second neighboring device was affected, while no nearest neighbor was influenced. Additionally, the cross-talk phenomenon appeared also during the set transition, which is mostly electric field-induced and not a purely thermal process. Additional investigation is required to verify whether thermal effects could be detrimental for data retention in our high-density array.

The observed cross-talk phenomenon is expected to occur only in applications based on a continuous switching medium. The integration of a continuous oxide film is however of crucial importance in many recent prototype applications of highly scaled ReRAM devices, based on both planar technology[37] or on a three-dimensional integration[15,16,47]. In the latter case in particular, the near proximity of the stacked cells make them particularly vulnerable to the cross-talk issue and it must be considered during the structure design. While the oxide patterning would provide a possible solution, it is responsible for a variety of additional issues related to the etching procedure and encapsulation[14], and is hardly applicable in case of stacked integration of vertical ReRAM devices.

CONCLUSIONS

A bottom-up fabrication approach based on BCP self-assembling allowed the fabrication of an ordered array of Pt/Ti/HfO_2/TiN resistive switching memory devices with a well-controlled diameter of 28 nm and a density of 5×10^{10} devices/cm^2, with further device downscaling possible. The bilayer Pt/Ti top metal electrodes were contacted using C-AFM, allowing a characterization of the device initial state variability, which was correlated with the inherent presence of the leakage current paths randomly spread in the HfO_2/TiN stack. The bipolar RS operation was confirmed for

the produced nanoscale devices, with a forming voltage lower than what is in general observed with the direct adoption of the AFM tip as top electrode. Owing to the high density of the nanodevices under study, we observed a cross-talk between two different memory cells at a distance of 75 nm, posing a potential issue for highly scaled, high-density memory applications based on continuous HfO_2 films. We ascribed the observed cross-talk to filamentary conduction paths in the oxide film, with different devices sharing a common portion of the filament.

METHODS

Substrate cleaning and bottom electrode processing. n^{++} Si wafers were cleaned by standard SC-2 ($HCl:H_2O_2:H_2O$ 1:1:5 solution) cleaning procedure; the native oxide was removed by 10s dip in HF solution (1:50), resulting in H-terminated Si. 10 nm Ti adhesion layer and 40 nm TiN as back electrode were afterward deposited by sputter deposition (100W RF power; 40 sccm Ar and 40sccm Ar/4sccm N_2 flux for the Ti and TiN depositions, respectively)

ALD HfO_2 oxide deposition. A 3 nm thick HfO_2 film was deposited on the bottom electrode by atomic layer deposition using Bis(methylcyclopentadienyl)methoxymethylhafnium(IV) (HfD-O4) and H_2O as precursors in the Savannah 200 ALD reactor (Cambridge Nanotech. Inc.) at 300°C substrate temperature.[48,49] Film thickness and dielectric properties were monitored by spectroscopic ellipsometry (Woolliam, Inc.).

Brush layer and block copolymer deposition. Samples were sonicated in an isopropanol bath prior to polymer deposition to remove particles contamination. A hydroxyl-terminated Poly(Styrene-r-Methyl methacrylate) random copolymer with molecular weight M_n = 14 kg mol^{-1}, Styrene fraction f 0.62 and polydispersivity index *PDI* 1.09 in a toluene solution (9 mg in 1 ml) was spun at 3000 rpm for 30s on the HfO_2 substrate for substrate neutralization and annealed at 310°C for 10min dwell time in an RTP machine (20°C s^{-1} ramp) in N_2 ambient (1000 sccm). A 5

min toluene bath removed the ungrafted polymer chains. A film of Polystyrene-b-Polymethylmethacrylate BCP (Polymer Source Inc.) was afterward spun on the neutralized surface. A toluene solution (9 mg in 1 ml) was used (M_n 101.5 kg mol^{-1}, f 0.67, *PDI* 1.07), spun on the surface at 3000 rpm for 30s. The self-assembling was promoted with a 250°C RTP annealing for 5 min in N_2 ambient. The final nanoporous PS template was obtained by removing the PMMA component with UV (5 mW cm^{-2}, λ 253.7 nm) for 15 min followed by a 100% acetic acid etch for 8 min, rinsing in water and drying in N_2 flow and a final oxygen plasma treatment at 40 W for a total of 130s.

Images of the samples surface were acquired with a FE-SEM (Supra 40, Carl Zeiss) at 15 kV using the in-lens detector.

Top electrodes nanopatterning. A film of 4 nm Ti / 6 nm Pt was deposited by electron-beam deposition on top of the nanoporous PS template, with a chamber pressure lower than $2\cdot10^{-6}$ mbar. The lift-off process was carried out in warm toluene (80°C, sonication bath).[19,27,28]

AFM electrical and morphological characterization. A Dimension Edge instrument (Bruker) equipped with a TUNA electrometer (1 pA – 1 μA current range) was used in combination with highly doped diamond-coated tips (CDT-CONTR, nanosensor, with 100-200 nm curvature radius but a nanoroughness in the 10 nm regime, lowering the contact area) or Pt/Ir coated tips (PPP-CONTPt, nanosensor, with a 25 nm thick coating on top of a <10 nm curvature radius tip). The bias voltage was applied to the substrate, while the tip was held grounded.

ASSOCIATED CONTENT

Supporting Information. Initial state conductance and device variability for two different sample areas; forming operations attempted using the Pt-Ir AFM tip as top electrode. This material is available free of charge via the Internet at http://pubs.acs.org.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript. ‡These authors contributed equally. (match statement to author names with a symbol)

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Any funds used to support the research of the manuscript should be placed here (per journal style).

Notes

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(Word Style "TD_Acknowledgments"). Generally the last paragraph of the paper is the place to acknowledge people, organizations, and financing (you may state grant numbers and sponsors here). Follow the journal's guidelines on what to include in the Acknowledgments section.

ABBREVIATIONS

CCR2, CC chemokine receptor 2; CCL2, CC chemokine ligand 2; CCR5, CC chemokine receptor 5; TLC, thin layer chromatography.

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