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# FPGA-based real time compensation method for medium voltage transducers

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## ABSTRACT

Since the increase of the distributed power connected to the medium voltage networks, a capillary monitoring of the power quality becomes essential. This entails the spread of transducers with suitable frequency bandwidths, as required by the relevant standards. The paper describes a real time compensation method for the extension of the frequency bandwidth of medium voltage dividers whose performances do not allow to perform measurements over a wide frequency range. This approach will contribute to keep the costs of this innovation low.

**Section:** RESEARCH PAPER

**Keywords:** voltage transducer, voltage measurement, power system measurement, power quality measurement, optimization

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## 1. INTRODUCTION

The growing need of power quality analysis in Medium Voltage (MV) grids, required by the increasing diffusion of distributed generation sources, has led to the employment of transducers and measurement techniques able to convert and acquire voltage signals with improved accuracy. Many applications require the use of transducers with wide frequency bandwidth ([1]-[3]), like power quality measurements ([4]), measurements on photovoltaic plants ([5]), energy and power meter calibration ([6]). For this purpose, voltage dividers which show higher frequency bandwidth and better linearity than conventional voltage transformers are becoming the most used transducers in power quality assessments. However, disadvantages like a higher dependency on the divider transfer function from environmental conditions (temperature, proximity effects) are introduced. The proximity effects can be reduced by shielding the device ([7]); this produces an increase of the stray capacitive coupling among the elements whose strength varies with the insulation medium. Many dividers,

for economic and safety reasons, make use of resin as an insulating medium whose electric characteristics can strongly depend on temperature, voltage and frequency ([8], [9]). With the aim of improving the performances of these dividers, so allowing their applications to grids with severe electrical and environmental conditions like the railway feed systems and on board MV circuits, a real time compensation method is proposed.

In scientific literature several papers face the issue of characterizing and compensating measurement instrument transformers ([10]-[16]). Most presented techniques perform compensation of measuring transformers only at industrial frequency; moreover, at best author's knowledge, none of them apply the compensation to transducers intended for medium voltage power systems. So, in this paper, an improved technique for compensating voltage transducers in a wide frequency range is presented. It is based on the identification of a digital filter, with frequency response equal to the inverse of the divider, which is executed on a Field Programmable Gate Array (FPGA), equipped with A/D and D/A converters. As an application, the transfer

function for the frequency compensation of two MV dividers is identified. The two chosen dividers have strongly different frequency behaviours; therefore the application of the proposed technique to the compensation of their frequency responses represents an interesting test bench.

The paper is organized as follows. In section 2 there is a description of the operation of the two dividers. In section 3 the measurement setup used to characterize the dividers is presented. Section 4 deals with the compensation technique. Section 5 presents the optimization results and finally section 6 shows the experimental results related to the compensated dividers.

## 2. DIVIDER FEATURES

The compensation technique is applied to two dividers with different frequency behaviour. One is a pure resistive divider (RD) and the other is a resistive-capacitive divider (RCD). The highest voltage for equipment ( $U_m$ ) is 24 kV for both. The resistive divider has a rated scale factor  $K_{NOM}$  of 10000 and a 30 M $\Omega$  high voltage arm. The RCD, whose  $K_{NOM}$  is 1000, is made, for the MV arm, of a series of 20 cells. Each cell consists of a 10 M $\Omega$  non-inductive thin film resistor ([8], [9]) and a 1.5 nF ceramic class 1 capacitor, parallel connected. For the low voltage arm an equivalent resistance of 155 k $\Omega$  and 116.4 nF ceramic capacitors are used.

The MV cells are disposed in four layers, each one made of five cells, which are series connected following an opposite path to minimize the stray inductances. A two sections cylindrical shield allows the control of the capacitive coupling due to the surrounding structures (Figure 1). Both the dividers are resin insulated, with a consequent downgrade of their performances. The transfer functions of the two dividers show strongly different dynamic behaviours (Figures 2 and 3). The scale factor and phase error of RD (Figure 2) have an overall variation of 30 dB and about 1.2 rad respectively over 4 decades, while the RCD (Figure 3) shows 12% and 100 mrad of variation over the same frequency range.

The so different frequency behaviour of the two dividers represents an interesting test bench for the compensation technique. In fact the identification of the parameters of the compensation transfer function requires a growing effort from RD to RCD.

## 3. DIVIDER CHARACTERIZATION

The complex frequency response of a voltage divider with a scale factor higher than 1000 requires a characterised measurement system able to compare voltage phasors whose amplitude differs three orders of magnitude. This can be performed by means of digitisers coupled with an attenuator probe or a reference divider, with high scale factor and frequency response up to at least 1 MHz. As an alternative, to perform the frequency sweep at low voltage (e.g. hundreds of volt), without making use of a reference voltage transducer, two Agilent 3458 multimeters (DMMs) are employed as digitizers. They have full scale ranges from

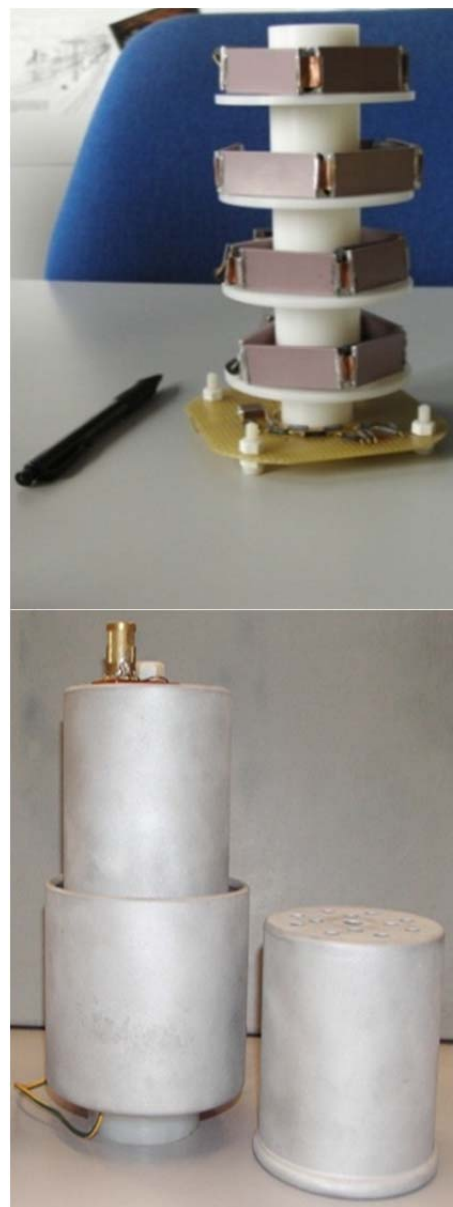


Figure 1. Resistive-capacitive shielded divider during the assembly step.

100 mV to 1000 V and a frequency bandwidth up to 12 MHz, depending on the selected digitizing technique. The synchronization between the two multimeters is provided by an external trigger supplied by a waveform generator. Before introducing the measurement circuit, some aspects on DMM digitizing methods are discussed in the following.

### 3.1. Multimeter digitizing methods

The multimeters provide three digitizing methods: DCV, Direct Sampling and Subsampling. Two of them, DCV and sub-sampling, are implemented for the divider frequency characterisation. By DCV technique, the signal is acquired just in DC mode, and the sample is obtained by integration of the input signal, over a specified integration time interval, that can be varied from 500 ns up to 1 s. The technique offers speed and resolution tradeoffs from 18 bits (5½ digits) at 6 kHz to 16 bits (4½ digits) at 100 kHz, as well a high input impedance. However, the maximum sample rate of 100 kHz associated with a bandwidth limited

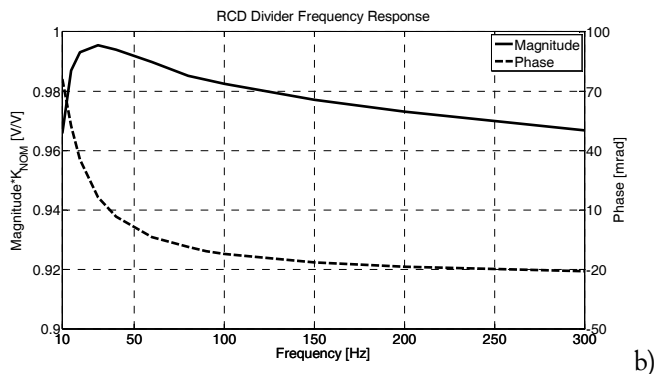
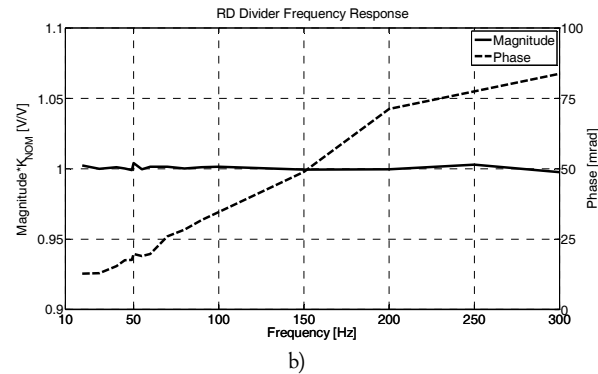
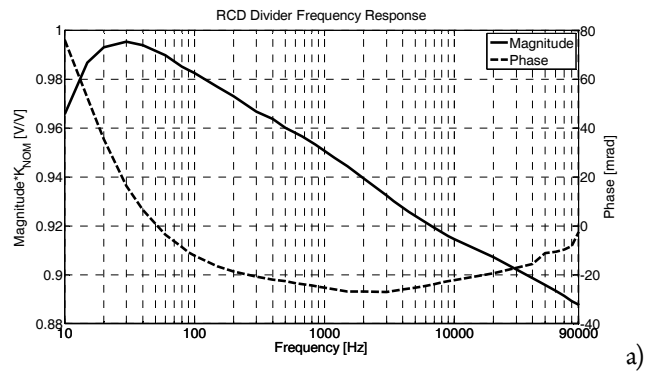
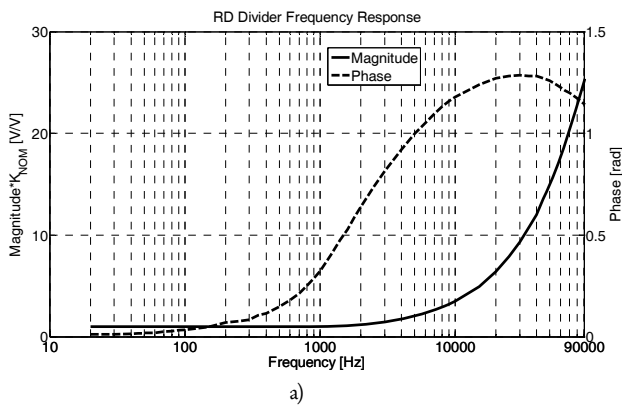


Figure 2. Frequency behaviour of RD divider between 20 Hz and 90 kHz (a) and zoom between 20 Hz and 300 Hz (b).

Figure 3. Frequency behaviour of RCD divider between 10 Hz and 90 kHz (a) and zoom between 10 Hz and 300 Hz (b).

to 30 kHz for 100 V and 1000 V full scale makes this digitizing technique not adequate to perform the frequency analysis up to 100 kHz, but it ensures a high magnitude and phase accuracy up to tens of hertz.

The sub-sampling technique employs a track and hold (T&H) circuit which performs the signal integration over a very small interval (2 ns) and holds the integrated sample during the slower A/D conversion.

The required A/D conversion time limits the actual sample frequency to 50 kHz, but thanks to the sub-sampling algorithm the sampling frequency reaches 100 MHz. The bandwidth at 100 V peak full scale is limited to  $1 \cdot 10^8$  V·Hz which means that at 100 V the bandwidth drops to 1 MHz. Table I summarizes the frequency bandwidth, the input impedance and the best accuracy for the employed scales and digitizing methods.

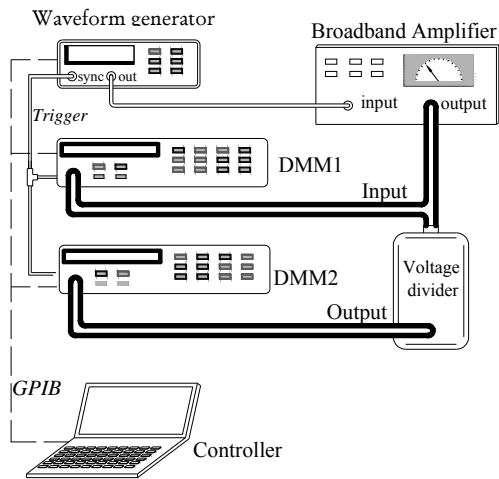
### 3.2. Measurement set-up

The measurement set-ups for the Subsampling and DCV digitising methods are shown in Figure 4a and 4b respectively. In both cases a waveform generator gives the trigger signal. For the DCV mode, a 5 V square wave signal triggers the simultaneous acquisitions of each sample by the two multimeters and the applied voltage is given by a power amplifier (DC – 500 kHz, 120 V) supplied by a calibrator.

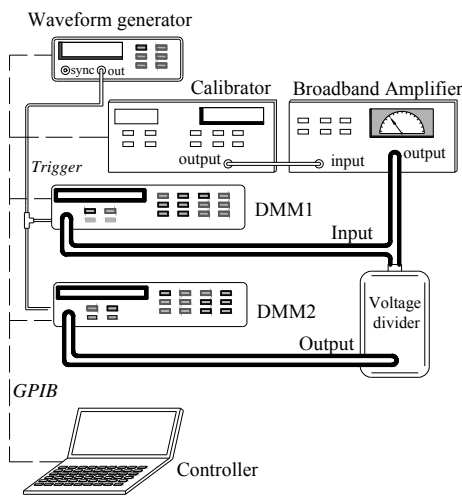
When the subsampling technique is used (a picture of this configuration is shown in Figure 5), the output of the waveform generator supplies the power amplifier and the available SYNC output triggers the two multimeter acquisition sequences. Since with this approach the multimeter time base is used, errors can be introduced because of slight differences in the two timebases.

Table 1. Multimeter specifications.

	Peak full scale	Bandwidth	Input impedance	Best Accuracy
DCV	100 mV	80 kHz	>1010 $\Omega$	0.00005 – 0.01%
	1 V	150 kHz	>1010 $\Omega$	
	100 V	30 kHz	>10 M $\Omega$	
	1000 V	30 kHz	>10 M $\Omega$	
Sub-Sampling	100 mV	12 MHz	1 M $\Omega$ 144 pF	0.02%
	1 V	12 MHz		
	100 V	12 MHz (1 MHz at 100 V)		



a)



b)

Figure 4. Measurement set-up for sub-sampling digitizing method (a) and for DCV method (b).

Because of its better accuracy at low frequency (within  $400 \mu\text{rad}$  up to some hundreds of hertz for the phase, when introducing corrections for the use of scales with different bandwidth), the DCV method is employed from 10 Hz to 60 Hz. As to the subsampling technique, a time delay of 25 ns, due to the different latency on the trigger for the two DMMs, becomes relevant in terms of angle for frequencies higher than 10 kHz. This systematic error is corrected but the overall accuracy degrades. Moreover, approaching 100 kHz the accuracy further decreases because of the bandwidth which is limited to 1 MHz for the 1000 V scale. For what concerns the uncertainty on the frequency of the generated signal, the utilized calibrator has an uncertainty of  $25 \text{ ppm} \pm 1 \text{ mHz}$  between 0.01 Hz and 11 kHz, while it has an uncertainty of  $25 \text{ ppm} \pm 15 \text{ mHz}$  between 12 kHz and 120 kHz. Summing up all the uncertainty contributions of the measurement setup, the measurement uncertainty is conservatively estimated to be 500 ppm and 5 mrad at 100 kHz for the scale factors and phase errors. The magnitude, phase and DC component of each voltage signal is estimated by the application of a fitting algorithm to the acquired samples over 10 periods. Since the

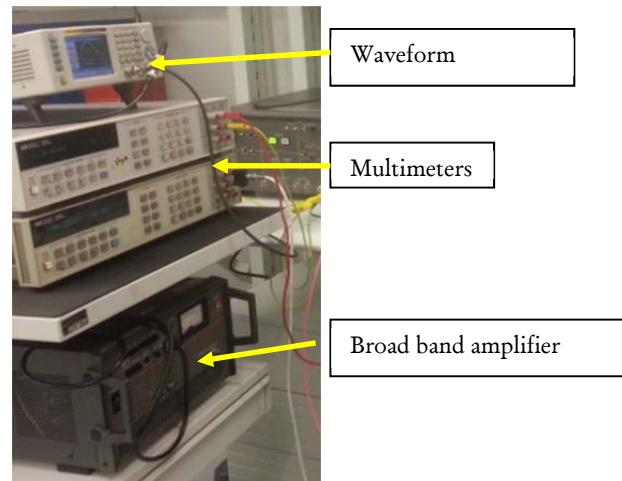


Figure 5. Measurement set-up for the Subsampling configuration.

waveform generator and the calibrator provides signals with very low distortions, no higher harmonics besides the DC and the fundamental one have to be inserted in the fitting procedure, which provides accurate estimation of the amplitude and phase within tens of ppm and microradians respectively.

#### 4. COMPENSATION TECHNIQUE

Since a divider can be considered as a linear system, its frequency response can be expressed by:

$$Y(f) = \frac{1}{R(f)e^{-j\varphi(f)}} X(f) \quad (1)$$

where  $X$  and  $Y$  are the spectra of the signals, both before and after the transduction.  $R$  and  $\varphi$  are systematic modifications introduced by the transduction in amplitude and in phase, respectively, on spectral components of the input signal.

Once the divider has been metrologically characterized and its frequency response found over a certain frequency range, cascading a device with a frequency response equal to the inverse of the divider frequency response, systematic deviations are compensated over all the considered frequency range. For this purpose, a filter can be adopted, whose frequency response,  $H_d(f)$ , should be exactly given by:

$$H_d(f) = R(f)e^{-j\varphi(f)} = \frac{X(f)}{Y(f)} \quad (2)$$

for any frequency,  $f$ , in the range of interest. The analog implementation of transfer function (2) is not easily practicable and it can lead to acceptable results only if applied to a very limited frequency range. Better results can be obtained with digital filtering. Obviously, for a real-time compensation, a digital processor has to implement such digital filtering. In the following the procedure for identifying the filter is described, while the hardware which executes it in real time is shown in the next sections.

Two main implementations for digital filters exist: FIR and IIR. FIR filters are relatively simple to compute and inherently stable but their main drawback, compared with

those of IIR filters, is that they may need a large number of coefficients to approximate a desired response; moreover they can only introduce a delay in phase frequency response. This makes them ineffective for the aim of this paper. An IIR filter is generally modeled by a transfer function in the  $z$ -domain that can be written as:

$$H(z) = \frac{b_0 + b_1 z^{-1} + \dots + b_m z^{-m}}{1 + a_1 z^{-1} + \dots + a_n z^{-n}}. \quad (3)$$

With this approach, filter design requires the choice of the best values for parameters  $a_1, \dots, a_n$  and  $b_0, b_1, \dots, b_m$  so that the transfer function of the filter approximates a desired frequency characteristic.

The problem of choosing the best coefficients can be formulated, from a mathematical point of view, as an inverse problem ([18], [19]) and solved by adopting optimization techniques ([16], [17]). An objective function, describing the difference among desired frequency response and obtained values has to be defined and minimized by an optimization algorithm. The choice of the objective (or cost) function affects the optimality and the computational complexity of the solution. A robust design should account for filter response over its entire bandwidth.

As illustrated in the previous section, the automated station used for divider characterization operates in the range of DC - 100 kHz: therefore, the best filter is identified in this range.

Anyway, identifying a filter, assigning frequency response data over its entire bandwidth, is a more complicated task, since its transfer function has fewer degrees of freedom. An efficient solution has been found choosing different expressions for filter transfer function and objective function. As it is said in [20], if the filter transfer function,  $H(z)$ , is factorized in second order sections (SOS), the frequency response is less sensitive to changes in coefficient values. This factorization can be expressed as:

$$H(z) = K \prod_{k=1}^N \frac{1 + b_{1,k} z^{-1} + b_{2,k} z^{-2}}{1 + a_{1,k} z^{-1} + a_{2,k} z^{-2}} \quad (4)$$

In addition, for the objective function ([21]), the following expression is used:

$$F(P) = \frac{1}{2} \sum_{i=1}^M W \cdot |\log_{10} H(f_i, P) - \log_{10} H_d(f_i)|^2 \cdot |\log_{10} f_{i+1} - \log_{10} f_{i-1}| \quad (5)$$

where  $P$  is the vector of the  $4N+1$  variables of (4),  $M$  is the number of the frequency points involved in the identification procedure and  $W$  is the vector of the weights. The cost function (5) weighs the ratio, rather than the difference, between the model frequency response and the frequency response data at each frequency. In addition, a logarithmically spaced frequency interval has been used. Practically it is like including Bode's concept in the cost function, in fact, it weighs the difference between Bode diagrams of the model frequency response and the frequency response data. It is important to note that this exactly addresses the real problem as what is really requested, it is to minimize the difference between the Bode diagrams obtained by the model and the experimental data.

The optimization problem here studied has a non-linear objective function with  $4N+1$  independent variables. Therefore, the research space should be  $R^{4N+1}$ , with  $R$  the whole set of real numbers. Nevertheless, this interval can be reduced adopting some constraints on solution characteristics. The constraints divide the research space into feasible and infeasible regions with remarkable reduction of computational burden ([22]). Considering this a constraint results in filter stability: the poles of the digital filter must have a modulus smaller than one, so nonlinear inequality constraints are imposed.

In order to numerically study equation (5), a hybrid scheme based on the combination of a stochastic and deterministic approach has been adopted ([23], [24]). The two approaches are used in a combined way to take advantages of their complementary characteristics. In fact, the deterministic approach is the fastest way to work out a solution but the quality of the results strongly depends on the choice of the starting point. Non-deterministic approaches do not depend on the initial choice and they are usually slow in finding out optimal solutions. Starting from these considerations, an initial exploration of space of solutions is made by a genetic algorithm having a population size greater than the number of coefficients chosen as target. Then, the obtained values are used as initial points to run a constrained deterministic approach based on the Sequential Quadratic Programming (SQP) ([22]) to find out the optimal solution. The SQP algorithm was preferred over simpler algorithms (such as zero-order methods) taking into account the information about the derivative of the objective function and, in addition, to include in a direct way the above mentioned constraints.

The described procedure has two parameters, which can be arbitrarily chosen before solution research starts: the sampling frequency and the number of SOSs.

Since the frequency response of the filter is strictly related to the sampling frequency, its value has to be carefully chosen. In fact, if the chosen sampling frequency differs from the actual sampling frequency of the utilized FPGA boards, then the actual frequency response of the executed filter differs from the one found in the identification procedure. For the case at hand, the utilized FPGA boards (described in detail in the next section) have a sampling period resolution equal to  $1 \mu s$ , while the timebase accuracy is equal to  $\pm 100$  ppm with a peak-to-peak jitter of 250 ps. According to such considerations, taking into account the frequency range involved in the compensation procedure, the sampling frequency has been chosen equal to 200 kHz.

The number of SOSs should be fixed very carefully because it is directly proportional to the number of independent variables of the objective function and to the complexity of the obtained filter. Typically, better results are obtained increasing the filter order. Anyway, it is fundamental to keep filter computational burden low. For this reason, the procedure is repeated a certain number of times, varying for each run the number of SOSs, in order to find out the best values for them.

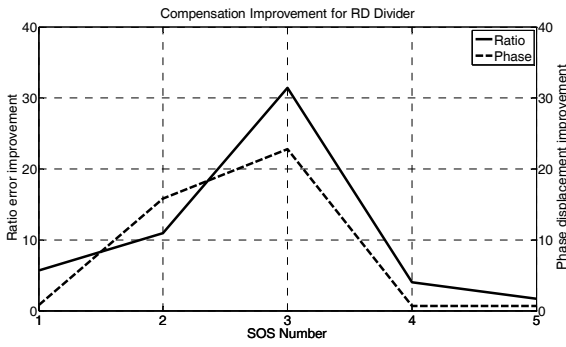


Figure 6. Compensation improvement for RD Divider.

The identification procedure is made in this way: first of all,  $H_d(f)$ , defined in (2), is constructed in a numerical way, linearly interpolating experimental data obtained from calibration. The optimization algorithm runs in two nested loops, varying the number of SOSs; in the inner loop the procedure is repeated a certain number of times. This is required based on the fact that the utilized hybrid optimization technique includes a stochastic algorithm which returns different results every run. The number of frequency points is chosen equal to four times the total number of variables [25]. Among the solutions, referring to the same number of SOSs and coming from the inner loop, the solution that minimizes the cost function is chosen.

### 5. OPTIMIZATION RESULTS

Data available from characterization of uncompensated dividers are used in the optimization procedure, in order to find the digital filters that, minimizing ratio error and phase displacement, could compensate the divider frequency response. As it is previously said, the sampling frequency of the digital filter is chosen equal to 200 kHz. The number of SOSs has been chosen from the range of 1 - 5. The reason of

this choice is that higher orders would require a high computational burden, not compatible with the hardware used for implementing the compensation filter. The inner loop is repeated 10 times. To evaluate the filter's performance, over the whole input frequencies range, ratio errors and phase displacements have to be evaluated before and after filter introduction. Those before the filter introduction are reported in (6) and (7), while those after the filter introduction are in (8) and (9), where  $H(f)$  is the frequency response of the implemented filter.

$$\Delta R(f_k) = 100 \left( \frac{1}{R(f_k)} - 1 \right) \quad (6)$$

$$\Delta \varphi(f_k) = \varphi(f_k) \quad (7)$$

$$\Delta R_c(f_k) = 100 \left( \frac{|H(f_k)|}{R(f_k)} - 1 \right) \quad (8)$$

$$\Delta \varphi_c(f_k) = \arg H(f_k) - \varphi(f_k) \quad (9)$$

Starting from the definitions (6)-(9), the two indices in (10) and (11) have been used for characterizing improvements introduced by the filter: they describe the relative mean quadratic improvements in ratio error and phase displacement, respectively.

$$I_R = \frac{\sqrt{\frac{1}{N_f} \sum_{k=1}^{N_f} [\Delta R(f_k)]^2}}{\sqrt{\frac{1}{N_f} \sum_{k=1}^{N_f} [\Delta R_c(f_k)]^2}} \quad (10)$$

$$I_\varphi = \frac{\sqrt{\frac{1}{N_f} \sum_{k=1}^{N_f} [\Delta \varphi(f_k)]^2}}{\sqrt{\frac{1}{N_f} \sum_{k=1}^{N_f} [\Delta \varphi_c(f_k)]^2}} \quad (11)$$

$I_R$  and  $I_\varphi$  are shown in Figure 6, for the RD divider, and in Figure 7, for the RCD divider, as functions of the number of SOSs.

For the RD divider, the improvements are about 31.4

Table 2. Coefficients of the best compensating filter for RD divider, expressed referring to the filter representation in (3).

<b>b0</b>	<b>b1</b>	<b>b2</b>	<b>b3</b>	<b>b4</b>	<b>b5</b>	<b>b6</b>
626.80	749.95	-415.10	-230.50	35.625	-4.3313	-6.7867
-	<b>a1</b>	<b>a2</b>	<b>a3</b>	<b>a4</b>	<b>a5</b>	<b>a6</b>
-	-0.46864	-0.96937	0.50844	0.0063371	-0.0026524	0.00017674

Table 3. Coefficients of the best compensating filter for RCD divider, expressed referring to the filter representation in (3).

<b>b0</b>	<b>b1</b>	<b>b2</b>	<b>b3</b>	<b>b4</b>
1111.8	-615.8	-1090.4	626.8	-9.1506
-	<b>a1</b>	<b>a2</b>	<b>a3</b>	<b>a4</b>
-	-0.53772	-0.98070	0.54920	-0.0078201

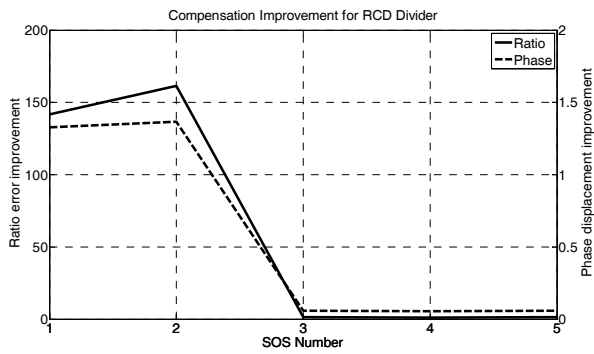


Figure 7. Compensation improvement for RCD Divider.

and 22.8 for ratio error and phase displacement, respectively. For the RCD divider, the improvements are about 161.4 and 1.4 for ratio error and phase displacement, respectively. Table 2 and Table 3 show the coefficients of the best compensating filters for, respectively, the RD and the RCD dividers; the coefficient refers to the standard representation for an IIR filter, that is the form (3).

## 6. EXPERIMENTAL RESULTS

In order to perform experimental verification of the filter, designed in the previous section, a compensating device has been implemented with a real-time digital processor, opportunely equipped with analog to digital and digital to analog converters.

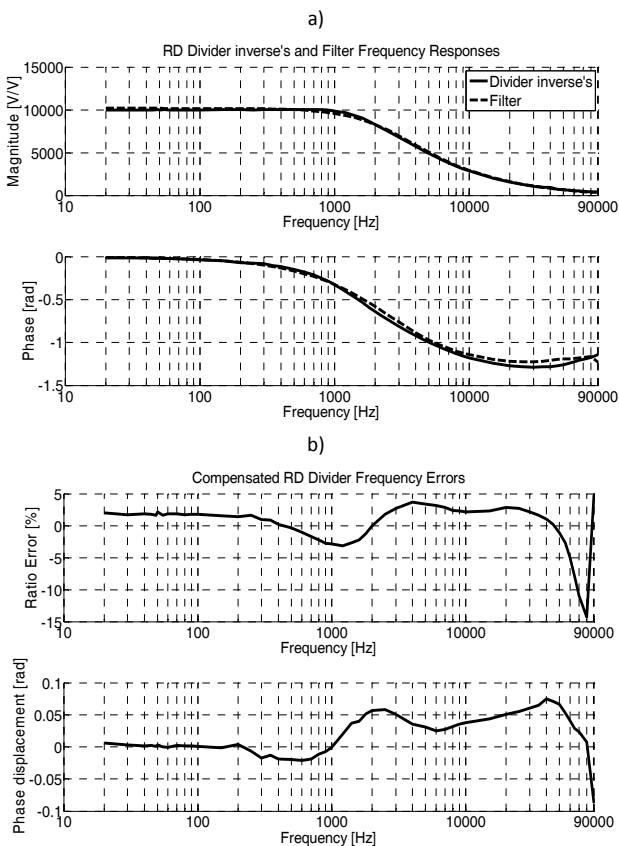


Figure 8. a) Inverse frequency response of RD divider and frequency response of its compensating filter. b) Ratio error and phase displacement of compensated RD divider.

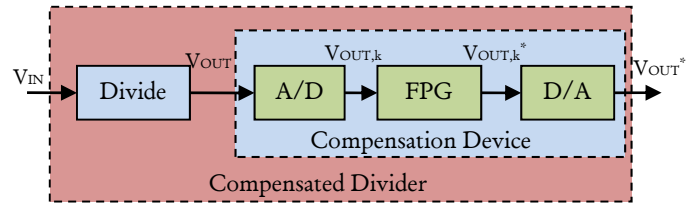


Figure 9. Block scheme of the compensated divider.

The case in question, an FPGA board has been used. Its features are: 1) Xilinx Virtex-II 1 megagate FPGA with 16 BUFGMUXs, 324 External IOBs, 227 LOCed IOBs, 40 MULT18X18s, 40 RAMB16s, 5120 SLICES [26]; 2) clock rate equal to 40 MHz; 3) 96 digital lines; 4) 8 analog inputs, independent sampling rates up to 200 kHz, 16-bit resolution,  $\pm 10$  V; 5) 8 analog outputs, independent update rates up to 1 MHz, 16-bit resolution,  $\pm 10$  V.

The block scheme of the compensated divider is shown in Figure 8, where  $V_{IN}$  is the input voltage,  $V_{OUT}$  the divider output voltage,  $V_{OUT,k}$  the sampled version of  $V_{OUT}$ ,  $V_{OUT,k}^*$  the filtered version of  $V_{OUT,k}$ ,  $V_{OUT}^*$  the analog version of  $V_{OUT,k}^*$  and it is the output of the compensated divider. In this way, the compensated divider continues to be an analog device, offering thus the possibility of being employed in whatever measuring system.

Using the presented compensation device, the two dividers were characterized through the measurement setup

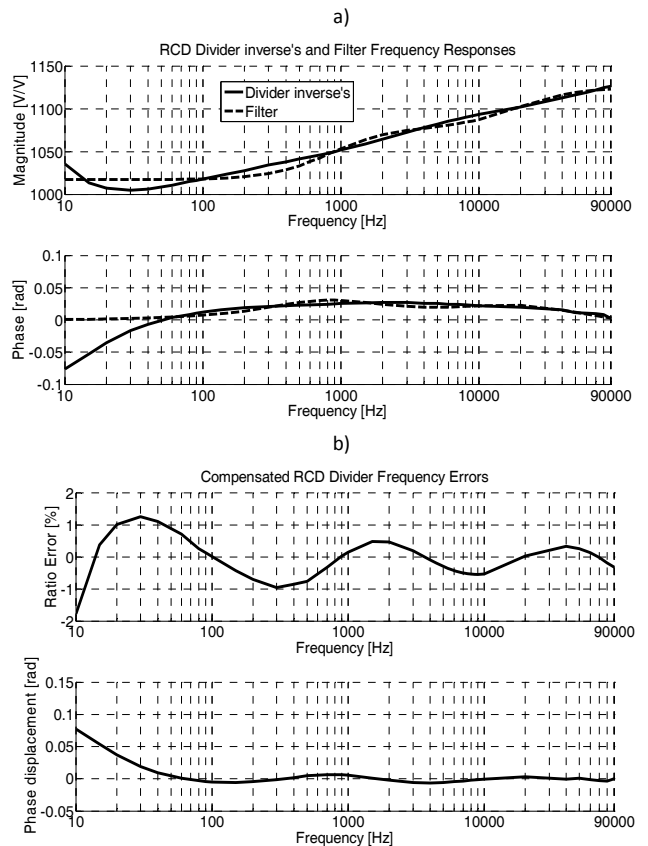


Figure 10 a). Inverse frequency response of RCD divider and frequency response of its compensating filter. b) Ratio error and phase displacement of compensated RCD divider.



shown in the previous sections. Figure 9 a) shows the RD divider inverses and its compensating filter frequency responses, while Figure 9 b) shows the ratio error and phase displacement of the compensated RD divider. Figure 10 a) shows the RCD divider inverses and its compensating filter frequency responses, while Figure 10 b) shows the ratio error and phase displacement of the compensated RCD divider.

## 7. CONCLUSIONS

Since the increase of the distributed power connected to the medium voltage networks, a capillary monitoring of the power quality becomes essential. This entails the spread of transducers with suitable frequency bandwidths, as required by the relevant standards. The paper describes a real time compensation method for the extension of the frequency bandwidth of MV voltage dividers whose performances would not have satisfied the requirements. The adoption of the compensation technique allows to reach improvement in dividers performance up to a factor 160. In this way, the performance of the compensated dividers is comparable with that of dividers of a better accuracy class, but the cost is kept low.

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